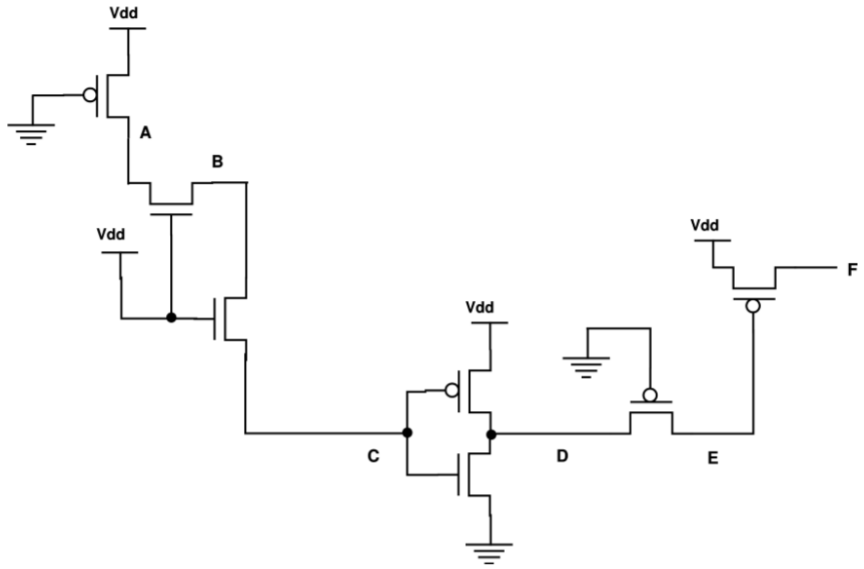
CME 342 QUIZ #2

This is an open book exam, the duration is 90 minutes. You need to scan and submit your work by end of the exam. The total points are 50.

1. (5 points) Find the voltages at each of the nodes, A, B, C, D, E and F below, assuming that all the nodes are initially at 2.5 V. Use the following circuit parameters.

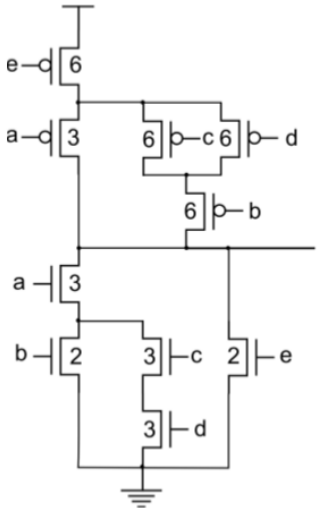
Vdd = 5V , Vtn = 0.5V , |Vtp| = 1.5V .



Answer:

A: B: C: D: E: F:

2. (10 points) The gate sizes of the transistors are given in the figure. Use the assumption that the diffusion capacitance is equal to the gate capacitance, and that a minimum sized transistor has gate and diffusion capacitance equal to *C*. The resistance of an nMOS transistor with unit width is R and the resistance of a pMOS transistor with width 2 is also *R*. Find out the logical effort of each input (a, b, c, d, e) and parasitic delay P.

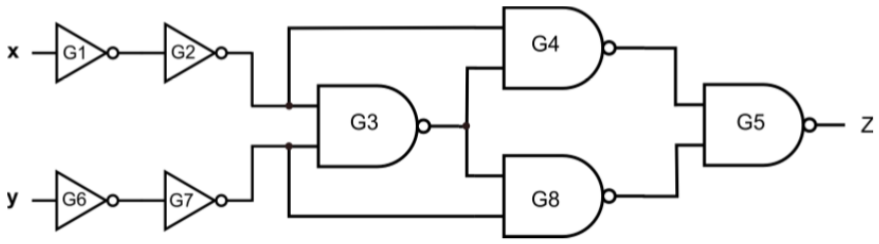


3. (10 points) A ring oscillator consisting of 15 minimum-sized (2:1) inverters in a loop, placed on a 45nm chip, has a measured frequency of 6.41 GHz.

(a) What is the delay of one stage of the oscillator?

(b) If the ring oscillator performance is assumed to be representative of the performance of the transistors on the chip, what would be the FO4 delay for the inverters in this particular chip?

4. (15 points) Given the 2-input Exclusive-OR circuit (with input buffers) below, input capacitance of inverter G1 = 3 units, and load capacitance driven by Gate G5 = 25 units.



(a) Calculate the delay of the path G1-G2-G3-G4-G5 in the diagram, using logical effort. Also give the sizes of the P and N transistors in each gate to achieve this delay. You may assume that the off-path capacitance is the same as the on-path capacitance for each branch.

(b) The assumption that off-path capacitance is the same as the on-path capacitance for each branch is probably true for the branch at the output of G3 (assuming the symmetric path is sized similarly), but probably not correct for the branch at the output of G2 (or G7, if that path is being sized). Suggest some way of improving the result above

5. (10 points) The following is an inverter layout in an 180nm process. Calculate the diffusion parasitic capacitance of the output B when input A is logic 1. Assume the substrate is grounded and Nwell is connected to VDD, which is 1.8V.

The width of the both PMOS and NMOS transistors are 0.5µm. The transistor characteristics for both NMOS and PMOS are CJ = 0.42fF/µm^2, MJ= 0.44, $CJSW$=0.33fF/µm, $MJSW$= 0.12, and ψ_0 = 0.98V at room temperature. Ignore the parasitic capacitance from the contacts.