

QUESTION #1

MARKS: 10 (2 + 2 + 2 + 2 + 2)

Indicate (in the space provided) whether the following are TRUE or FALSE. Include a SHORT sentence in support of your answer. Do any FIVE (5).

Please note that each INCORRECT answer will be penalized 1 mark.

F-1) Device Well, diffusion, and thinox all refer to the same thing.

False F 2) The 3 in CMOS3DLM refers to the minimum layout feature size. The 3 means the actual minimum feature size is 3µm. Min layout size is 5µm.

False F 3) Circuits designed by the University of Saskatchewan are fabricated by the Canadian Microelectronics Corporation (CMC) in Kingston, Ontario. They are fabricated by Northern Integ (BNR) in Oshawa, Ontario.

True 4) Bipolar CMOS (BiCMOS) is the technology of the future. This technology is currently being researched. Near future.

False F 5) Field oxide (FOX) exists everywhere that thin oxide (TOX) doesn't. FOX can exist over top of TOX at the end of the process. WHEN? in structural. FOX and TOX don't exist in the same time.

True 6) The Metal2-Via enclosure rule is larger than the Metal1-Contact enclosure rule. The Metal2-Via enclosure rule is 3µm and the Metal1-Contact enclosure rule is 2µm.

Name: [redacted] - 2 - Student Number: [redacted]

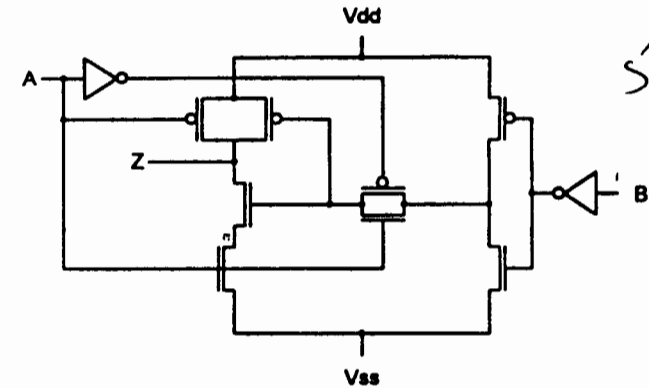
QUESTION #2

MARKS: 15 (5 + 10)

The circuit shown in the circuit schematic below serves a useful purpose.

a) Determine the logical function of the circuit. A truth table below should be used for this purpose. What standard function, if any, does this circuit perform?

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0



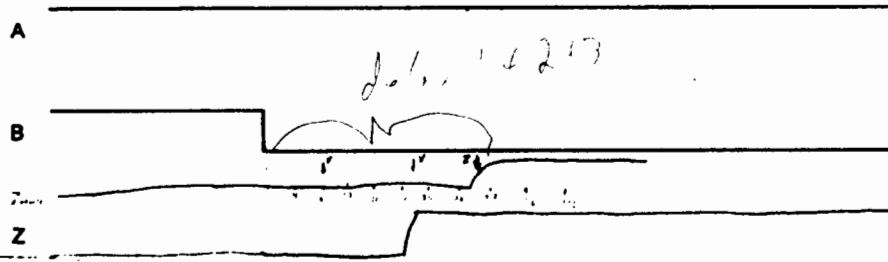
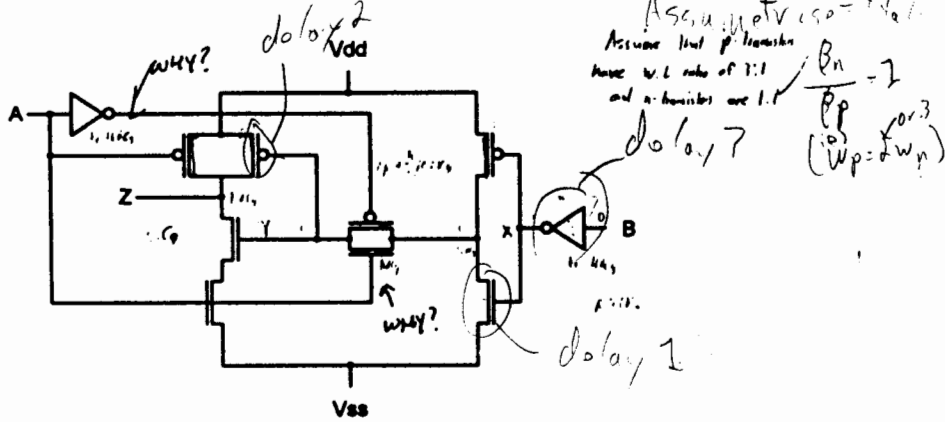
This performs a standard NAND function.

Name: [redacted] - 3 - Student Number: [redacted]

"The reason why we have midterms is not because we're not allowed to extract your fingernails with a pincer."

b) The circuit schematic from Part a) is shown below. For the input waveforms shown, what is the approximate delay time from the B input going low (V<sub>DD</sub> volts to V<sub>SS</sub> volts, 2ns fall time) and the Z output changing level?

State any assumptions that you make. All assumptions must be valid and have some basis in fact.



Assumptions:  
 All gate number to 100  
 100% fanout  
 100% fanout  
 100% fanout  
 100% fanout

How?  
 5  
 delay 1: 100ns  
 delay 2: 100ns  
 delay 3: 100ns  
 delay 4: 100ns  
 delay 5: 100ns  
 delay 6: 100ns  
 delay 7: 100ns  
 delay 8: 100ns  
 delay 9: 100ns  
 delay 10: 100ns  
 delay 11: 100ns  
 delay 12: 100ns  
 delay 13: 100ns  
 delay 14: 100ns  
 delay 15: 100ns  
 delay 16: 100ns  
 delay 17: 100ns  
 delay 18: 100ns  
 delay 19: 100ns  
 delay 20: 100ns  
 delay 21: 100ns  
 delay 22: 100ns  
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 delay 90: 100ns  
 delay 91: 100ns  
 delay 92: 100ns  
 delay 93: 100ns  
 delay 94: 100ns  
 delay 95: 100ns  
 delay 96: 100ns  
 delay 97: 100ns  
 delay 98: 100ns  
 delay 99: 100ns  
 delay 100: 100ns

Name: \_\_\_\_\_ Student Number: \_\_\_\_\_

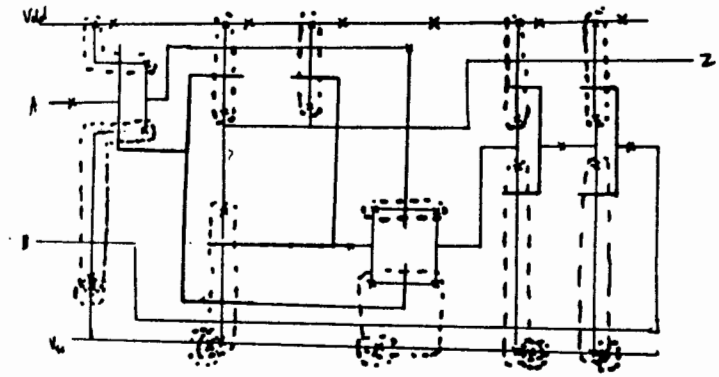
QUESTION #3

MARKS: 20 (20)

a) From the circuit schematic shown in Question #2 Parts a) and b) draw a STICKS diagram for the circuit.

You must use the following constraints in drawing your STICKS diagram:

- Use E.E. 451.3 standard STICK colors and patterns.
- Show p+ and P-well. Do not show p-guard or N-well.
- A and B must come in from the same side. Z must leave from the other side. Label the input and output lines.
- No interconnection layers are allowed to lie outside the V<sub>DD</sub> and V<sub>SS</sub> power supply rails.
- At least one (1) V<sub>DD</sub> substrate contact and one (1) V<sub>SS</sub> substrate contact must be shown.



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Name: \_\_\_\_\_ Student Number: \_\_\_\_\_

"No, no, no... let me ask someone who doesn't know so I can scream at them."

Midterm 1994

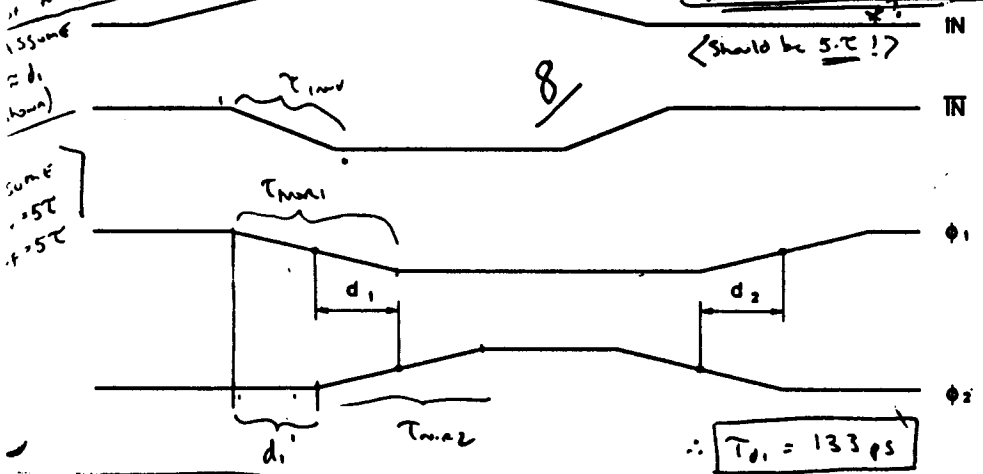
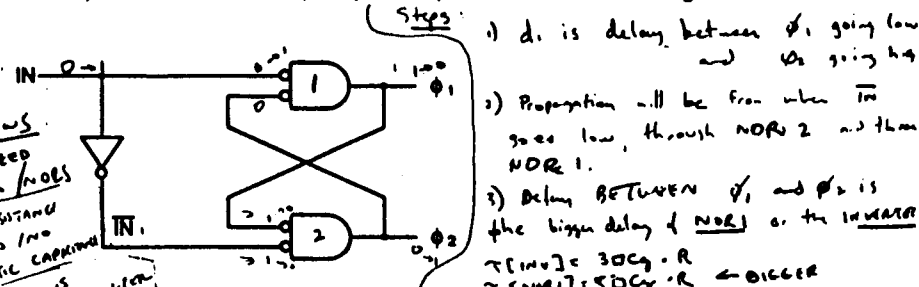
The following circuit serves a useful purpose. It was discussed in class.

- a) Determine the dead zone time ( $d_1$  or  $d_2$ , pick either one, your choice). Representative waveforms are shown below.

State any assumption(s) that you make. I might suggest two (2) that will make your task easier:

- 1) Assume linear rise and fall times, even though you may be using exponential waveforms.
- 2) Assume constant pull-up and/or pull-down resistance during transitions.

ASSUMPTIONS:  
mid-sized inverters / NORs  
NO RESISTANCE WIRE IN PARASITIC CAPACITANCE  
SAME INPUT IS MISSED INVERTER

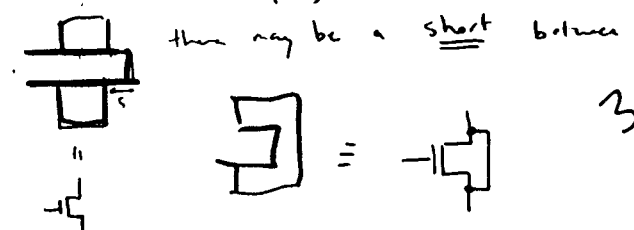


(about midterm marks) "I have to use the Wonder-Bra method: push it up as much as you can!"

Explain briefly, but as completely as possible, FIVE (5) of the following. A SHORT paragraph should be sufficient.

- a) Design rule E.1 concerns the overlap of Poly over Device Well (see Appendix C: Available Process Technologies, page C9). It is given as 5 design scale microns (5 $\mu$ m). What is the basis for this rule?

If poly does not completely overlap the diffusion, there may be a short between Drain and Source:



- b) Using CMOS technology complicates the fabrication process (with respect to nMOS). Give TWO (2) advantages of CMOS (with respect to nMOS). Give ONE (1) disadvantage of CMOS (with respect to nMOS).

ADVANTAGES of CMOS:

- 1) Rise and fall times are of the same order. (vs rise time is slower than fall for nMOS)
- 2) Almost zero static power dissipation.

DISADVANTAGES:

- 1) Requires 2N devices for N inputs (vs N+1 devices for nMOS)
- 2) Where is the Canadian Microelectronics Corporation (CMC) located? Who does their fabrication? Where are they located?

CMC located at Queen's University in Kingston, ONTARIO.

Fabrication is by Northern Telecom located in Ottawa, Ontario.

d) Technically speaking, is the circuit shown in Question #1 of this examination paper level-activated or edge-triggered? Is it a latch or a flip-flop? Explain.

- LEVEL ACTIVATED, OUTPUT CHANGES ON BOTH EDGES  
 THEREFORE IT IS NOT EDGE TRIGGERED  
 - NO MEMORY,  $\therefore$  NOT A FLIP FLOP  
 - OUTPUT FOLLOWS INPUT (COMPLEMENT),  $\therefore$  LATCH

e) List THREE (3) ELECTRIC™ keyboard commands that you have used. Give a SHORT description of each one.

- 1) - help <x>: Will show a short description of command x, if one is available
- 2) - tellaid simulation <x>: Selects ELECTRIC to prepare a simulation for x (x is usually esim or spice)
- 3) - onaid simulation: Tells ELECTRIC to begin simulation preparation for the package specified in "tellaid simulation <x>"

f) What is the essential difference between Gate Array design and Field Programmable Gate Array design? Which one is "better" (define "better" in your answer)?

Gate Array: Can only be "mask-programmed": I.E. is "PROGRAMMED" AT THE FABRICATION SITE, BY FABRICATORS.

FPGAs: CAN BE "FIELD PROGRAMMED" BY THE DESIGNERS. (AT THE DESIGN SITE).

FPGAs are "BETTER", if BETTER means quicker turnaround time, cheaper and easier to debug designs.

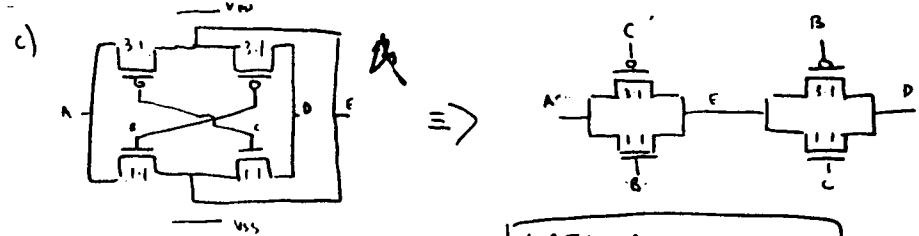
QUESTION #3

MARKS: 20 (8 + 3 + 4 + 5)

It is desirable for VLSI designers to "reverse engineer" circuits that have been created by other VLSI designers. In this way you can see other ways of doing the "obvious" and thereby learn new techniques that can be used in circumstances that may arise in your personal integrated circuit designs, such as on examinations.

- a) Shown on the next page is a standard cell for a useful logic design function. From the Laser\_plot plot of the cell determine the STICKS diagram for the circuit. This may be done by "coloring" the Laser\_plot. Where appropriate, "Coloring" may consist of a single line down the center of each layer polygon that is visible. Make sure that you use EE 451.3 standard colors.
- b) How many split-contact cuts are there in the Laser\_plot? Normal contact cuts? Vias?
- c) From the STICKS diagram determine the circuit schematic (i.e., the transistor layout and interconnection) for the circuit. Make sure you show the transistor sizes in the circuit schematic (use W:L). Label the inputs and outputs.
- d) From the circuit schematic determine the truth-table for the circuit. Note potential problems with this circuit (if any).

b) There are NO (zero) split contacts  
 There are FOURTEEN contact cuts  
 There are FIVE vias



ASSUME: TENTH TABLE VALUES GIVEN AT STEADY STATE

d)

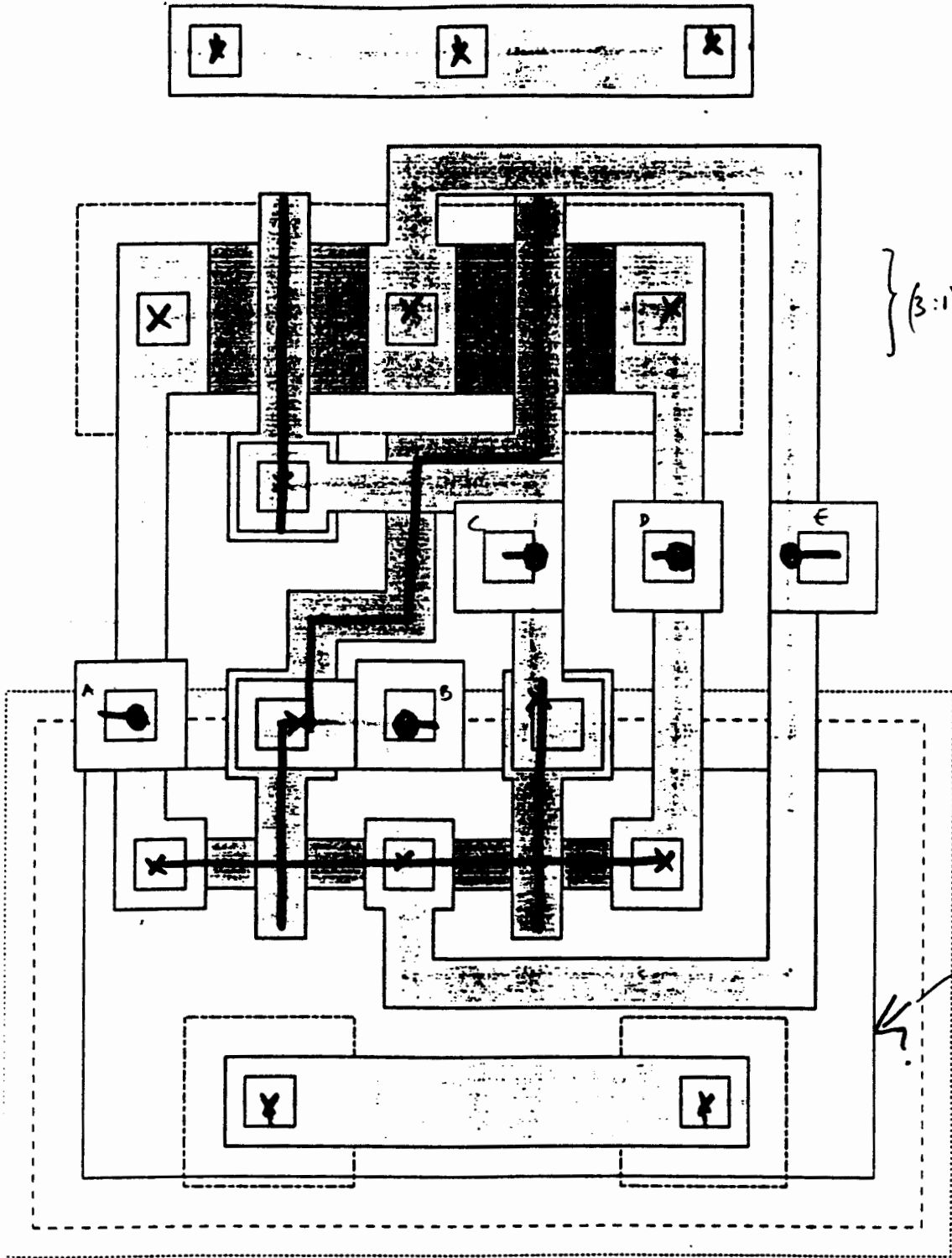
A	B	C	D	E	(A' LAST A) (E' LAST E)
0	0	0	0	0	
0	0	1	E'	A'	
0	1	0	E'	A'	
0	1	1	0	0	
1	0	0	0	1	
1	0	1	E'	A'	
1	1	0	E'	A'	
1	1	1	1	1	

INPUTS: A  
 "2<sup>nd</sup> CLOCK" INPUTS: B, C  
 OUTPUTS: E, D

Potential Problems:  
 1) If B and C are NOT complementary then the circuit will propagate different values at different speeds (i.e. for B=C=0 or B=C=1) to E.  
 2) if B and C overlap on 0 or 1, signal A will propagate through to D (to transparent)

"This means that everyone who was alive and halfway breathing and not thinking about sex got it right."

Laser\_plot



(3:1)

p-well (arrow)

- = METAL 2

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