EE 391 (All Sections)

Midterm Examination

Tuesday, October 31, 2006

Time Allowed: 2 Hours

Materials allowed: Laboratory Notebooks, Calculators

Instructions:

- **Answer all questions in the space provided (use page backs for rough work if necessary)**
- **State your assumptions; show all relevant work. Box, circle or otherwise highlight your answers where appropriate. For multiple choice, circle the correct answer.**
- ***Put your name and student number on each page; (we may separate them for marking purposes)***
- **Refer to the last page for relevant product data when required**
- **Weighting for each question is indicated in the left margin (Total marks: 120)**

(Marker's use only.)

S. L.	Noise	Op A	Fourier	2nd Ord	FET	Total
15 /20	/21	/19	/20	/20	/20	85 /120

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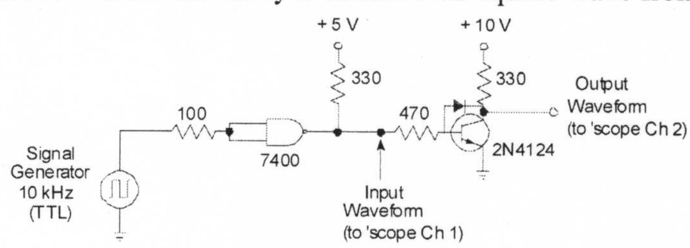
Timing in Sequential Logic

Q1.1) **[3]** In general, a ring of N inverters with an average propagation delay of t_p, will oscillate with a frequency of ___1/2Ntp___ and a period of ___2Ntp___. N must be (odd) / even (circle one) number of inverters.

Q1.2) Consider the basic inverter circuit shown below driven by a 10kHz TTL square wave from the signal generator.



The oscilloscope trace of the input and output waveforms are shown at right. Determine the values of the following parameters *if shown*, and label them on the 'scope figure.

[6]

i) t_r ___300ns___

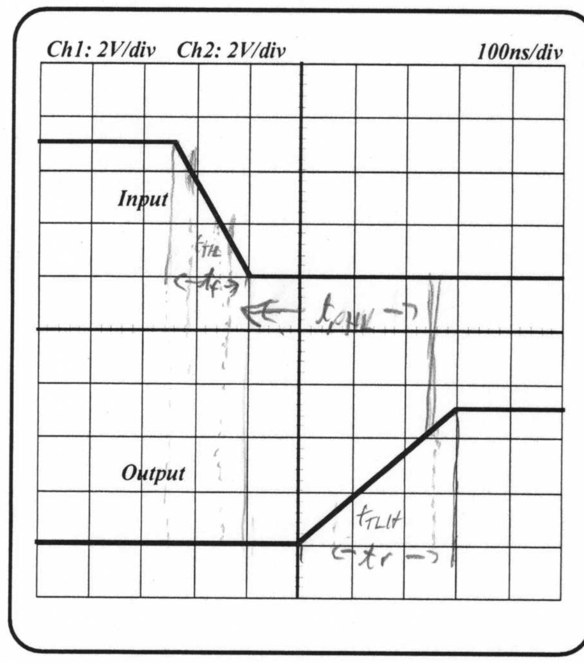
ii) t_f ___150nS___

iii) t_{PLH} ___400nS___

iv) t_{PHL} ___Not shown___

v) t_{THL} ___50nS___

vi) t_{TLH} ___200nS___



4

Q1.3) Design a simple astable oscillator using a single 4069 Hex-inverter chip so that it could be used as a clock source for a counter circuit. Show *all* the necessary wiring connections on the drawing below. Design for a clock frequency of approximately 2.35MHz (Assuming "typical" operation).

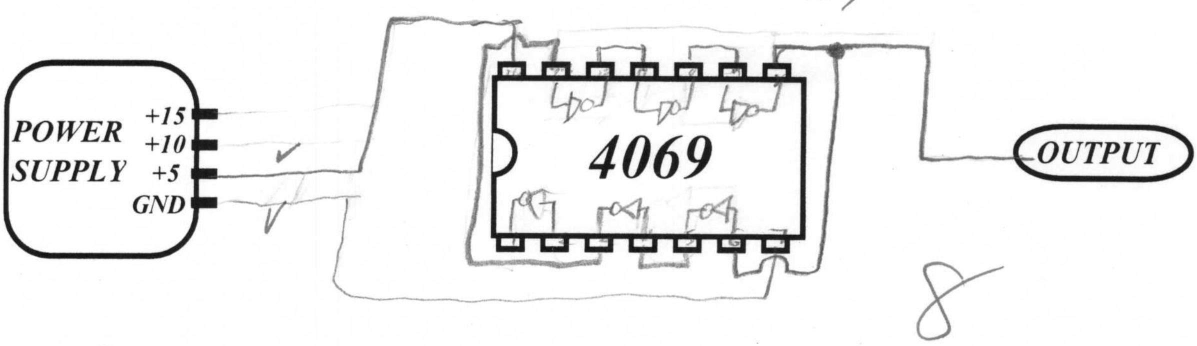
[8]

$f = 2.35MHz$ $T = \frac{1}{f} = 425nS$ $t_p \approx 45nS$ @ +5V

$T = 2Nt_p$

$425 = 2N(45.5)$

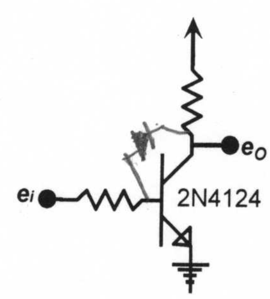
$N = 5$ (must be odd # to oscillate)



8

Q1.4) Indicate the correct placement of a bypass diode on the simple transistor inverter shown in the accompanying diagram.

[1]



Q1.5) Why is propagation delay reduced with a speed-up capacitor?

[1]

The capacitor sucks off carriers from the base as the capacitor is charged and it helps de saturate the transistor.

Q1.6) The large capacitance associated with a 1:1 probe causes a _increase / decrease_ propagation delay resulting in a __higher / lower_ oscillating frequency (circle the correct response).

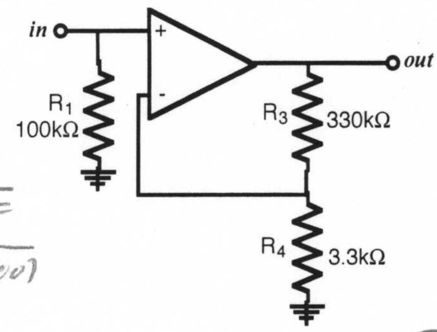
[1]

11

Noise Sources and Virtual Instruments

Q2.1) a)

Calculate the Noise Factor and Noise Figure for the op-amp-based amplifier shown at right if the noise observed at the output of the amp with a HP3580A Spectrum Analyzer is -85.5dB$_V$. There were no other components connected to the input at the time of measurement.. The resolution bandwidth of the Analyzer was set to 100Hz and the temperature is 300^{0}K. You can assume that the noise current density for the op amp is $i_n = .01 \frac{pA}{\sqrt{Hz}}$.



[7]

$V_{rms_o} = 53.1\mu V = N_A + N_i$

$N_i = 1.28\times10^{-10}\sqrt{R\Delta f}$
$= 1.28\times10^{-10}\sqrt{(100k)(100)}$
$= 0.404\mu V$

Noise factor $\frac{53.1\mu V}{0.404\mu V} = 131$

Noise figure $= 10\cdot\log$ (Noise factor)
$= 21.2$

3

b)

How does this compare to the noise factors/figures you calculated for the amplifiers you tested in the lab? Is this a better or poorer amplifier from a noise perspective?

These are smaller than our noise factors/figures. This is a better amplifier from a Noise perspective.

2

Q2.2) When measuring the noise from an external resistor, you note a reading on the spectrum analyzer of -71dB$_V$. While you are recording the reading in your log book, your partner changes the resolution bandwidth to 30Hz and the reading changes to -76.3dB. What resolution bandwidth was selected before?

[4]

$30\times5 = 150$ Hz

$V_{ne}^2 = 4kTR\Delta f$ = ↑ in V_{nf} by 5 ↑ in Δf by ×5.

2

Q2.3) A 50kΩ resistor is connected to the terminals of the HP 3580A Spectrum Analyzer. With the resolution bandwidth set to 100Hz, you observe a reading of -127dB$_V$. What is the noise floor of the spectrum analyzer? Assume that the temperature conditions are approximately 300^{0}K, and the reading is taken at a low enough frequency so the internal capacitance of the analyzer is not a factor.

$V_{rms} = 1.28\times10^{-10}\sqrt{R\Delta f}$
$= 1.28\times10^{-10}\sqrt{(50k)(100)}$

[4]

$= 90.5\times10^{-9}$

$20\cdot\log(90.5\times10^{-9}) = -140.9$ dB

1

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