

Mid-Term Examination

Name: Shea Pederson

Student ID: 10288579

- 2 Hours. No materials allowed. [Number] indicates weighting
- No interaction with another student is allowed during the exam. Cheating will not be tolerated.

1. Which one is not related to RISC? [0.5] *Reduced in*

a) as few lines as possible *✓*

b) pipelining is possible *← seems complex*

c) simple instructions *✓*

d) each instruction requires one clock cycle to execute *✓*

$$\frac{27.75}{30} = 92.5\%$$

$$\frac{2.25}{30}$$

2. Which one is not related to Von Neumann architecture? [0.5]

a) same memory holds data, instructions *✓*

b) a single set of address/data buses between CPU and memory *✓*

c) simpler than Harvard architecture *✓*

d) allows two simultaneous memory fetches

3. What is the difference between FFs and Latches? [1]

FFs are edge sensitive

Latches are level sensitive

00	0
01	0
10	1
11	1

toogles

4. What is the major advantage of Floating-point number system over Fixed-point number system? [1]

Increased range. The accuracy can be focused about any point on the number line (within the exponent range)

5. IC manufacturers utilize address multiplexing technique. What is address multiplexing and what is the main purpose of using it? [1]

Multiplexing stores a given number in less lines. It allows full use of the address lines instead of having a dedicated line per address.

6. Assume that the following operands are initially stored in data memory: [C350] = 0F, [C351] = 01, [C352] = FF. [4]

```

C300 B6 ;LDAA
C301 C3
C302 50
C303 B0 ;SUBA
C304 C3
C305 51
C306 27 ;BEQ
C307 03
C308 B7 ;STAA [C352] = 0E
C309 C3
C30A 52
C30B 3E ;WAI
C30C ??

```

Assuming SUBA $\rightarrow A = A - (\text{address value})$

A = 0F

$$A = \frac{0F}{0E}$$

$$A = \frac{0F}{0}$$

(a) What will be [A] and [C352] at the completion of the program?

$[A] = [C352] = 0E$

(b) Assume that [C351] = 0F initially and repeat (a). $[A] = 0, [C352] = FF$

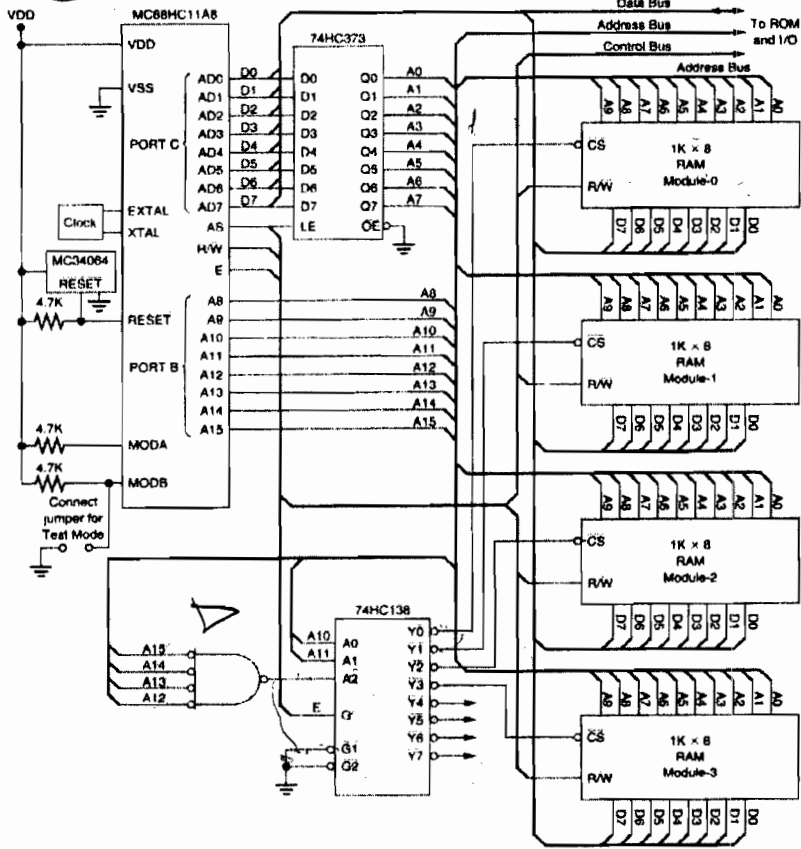
7. What tells the microprocessor unit whether or not it is supposed to fetch an operand address as part of an instruction? [1]

op code. The op code is latched into the IR. The timing and decoding circuitry decodes the op code \rightarrow from there it know whether or not to fetch an operand address.

this #8 will be on final!

8 4 2 1

8. Refer the following figures. What is the occupying address for each module? Show your way to minimize the decoding circuitry. Discuss your scheme's advantage and disadvantage. In your new scheme, how many address ranges can MPU use to access module-0? What are they? [5]



Current Change
 MOD-0 -> 0000-03FF
 MOD-1 -> 0400-07FF
 MOD-2 -> 0800-0BFF
 MOD-3 -> 0C00-0FFF

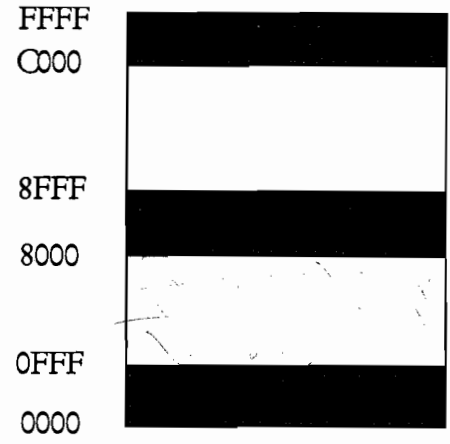
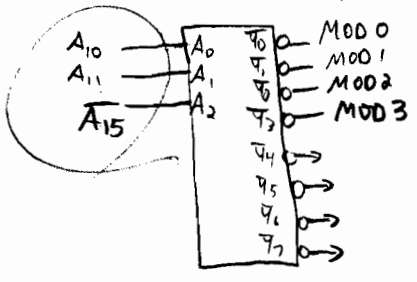


FIGURE 5.14 Typical RAM decoding logic in a 68HC11-based MPU.

Use partial decoding to minimize logic.

To CS on:

0xxx ——— *to all chips*



For MOD 0
0xxx 00 ——— *to all chips*
 Address ranges MOD 0

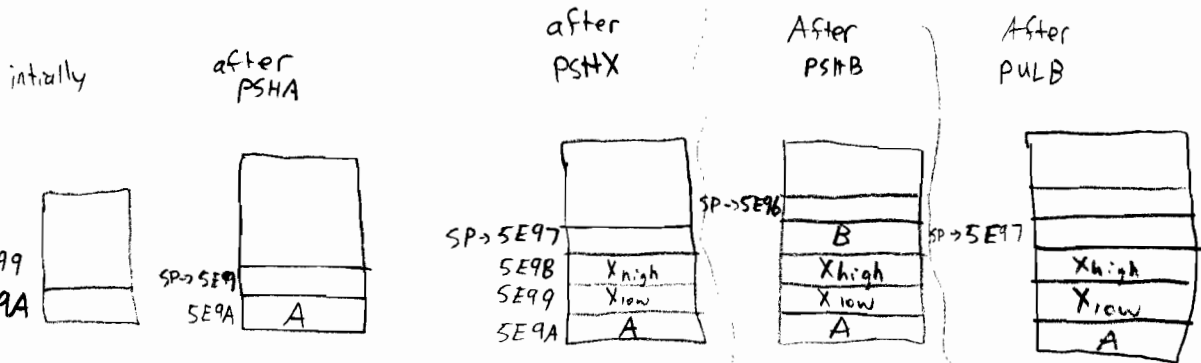
- 0000 - 03FF
- 1000 - 13FF
- 2000 - 23FF
- 3000 - 33FF
- 4000 - 43FF
- 5000 - 53FF
- 6000 - 63FF
- 7000 - 73FF

8 ranges total

Using this new scheme (partial decoding), it minimizes decoding logic. The downside is that you give up addresses (memory capacity) since there are 8 addresses that point to the exact same physical location.

9. Consider the following program and assume that the stack pointer register is initially with 5E9A₁₆. Show the contents of the stack after each instruction. What are the contents of the stack pointer register at the end of the execution of the three push instructions. [5]

PSHA, PSHX, PSHB, PULB



[SP] = 5E97 @ end

10. Each of the following is an assembly language instruction that will load data into accumulator A. For each, indicate where the data comes from and the type of addressing mode. Assume that $[X] = 0200_{16}$. [5]

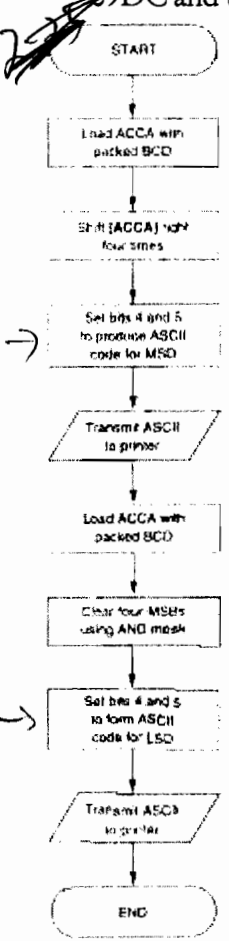
- (a) LDAA #2D (Immediate. Data is $2D_{16}$. It comes directly from the code.)
- (b) LDAA \$1234 (Extended. Data comes from address 1234)
- (c) LDAA \$7C (Direct. Data comes from address 007C)
- (d) LDAA \$3F, X (Indexed. Data comes from address $023F$)
 $X + 3F = 023F$
- (e) LDAA #64 (Immediate. Data is 64_{10} .)

11. Discuss the relative advantages and disadvantages of direct and extended addressing. [1]

Direct → requires less bytes to execute (only one byte needed for address)
 → But, cannot address anything outside of (0000 - 00FF)

Extended → requires 2 bytes for address
 → But can address a larger range: (0000 - FFFF)

12. Write the program for BCD-to-ASCII conversion flowchart. Assume that the packed BCD is in memory location 09DC and the printer output port is at address 7C00. Refer the following descriptions of instruction sets. [5]



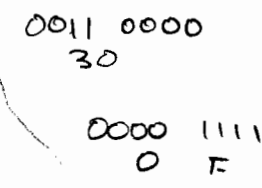
```
(0.25) LDAA $09DC
      LSRA ; shift ACCA right
      LSRA ; (4 times)
      LSRA
      LSRA
```

```
(0.75) LDAB #$30 ; load OR mask
      STAB $09DB ; store OR mask
      ORAA $09DB ; OR A, $30. Store result in A.
```

```
(0.75) STAA $7C00 ; send to printer
(0.25) LDAA $09DC ; load packed BCD
      LDAB #$0F ; load AND mask
      STAB $09DB ; store AND mask
      ANDA $09DB ; AND A & 0F. Store result in A
```

```
LDAB #$30 ; load OR mask
STAB #$09DB ; store OR mask
ORAA $09DB ; OR A, $30 store result in A
```

```
(0.5) STAA $7C00 ; send to printer
(0.25) WAI ; wait for interrupt.
```



- AND: Logical AND
- ASL: Arithmetic Shift Left
- CBA: Compare Accumulators
- DEC: Decrement
- EOR: Exclusive OR
- INC: Increment
- JMP: Jump
- LDA: Load Accumulator
- LSR: Logical Shift Right
- ORA: Inclusive-OR
- ROR: Rotate Right
- STA: Store Accumulator
- SUB: Subtract
- TBA: Transfer from Accumulator B to Accumulator A
- WAI: Wait for Interrupt

I realized this code is bulky. I forgot the syntax to OR/AND a mask directly with the ACCX, instead of using temporary memory.

THE END
 Good Luck to other exams!

